IEEE VLSI Based projects based on verilog and Xilinx.

Image Processing

1. **Implementation of Canny Edge Detection Algorithm on FPGA and displaying Image through VGA Interface**
   Edge detection is one of the most important stages in image processing. The Canny edge detection algorithm is most widely used edge detection algorithm because of it advantages. In this paper we present canny edge detection algorithm implemented on Spartan 3E FPGA and developed VGA interfacing for displaying images on the screen. In this paper we have taken 128×128 Image and displayed same on the monitor through FPGA.

2. **A Low-Cost VLSI Implementation for Efficient Removal of Impulse Noise**
   Image and video signals might be corrupted by impulse noise in the process of signal acquisition and transmission. In this paper, an efficient VLSI implementation for removing impulse noise is presented. Our extensive experimental results show that the proposed technique preserves the edge features and obtains excellent performances in terms of quantitative evaluation and visual quality. The design requires only low computational complexity and two line memory buffers. Its hardware cost is quite low. Compared with previous VLSI implementations, our design achieves better image quality with less hardware cost. Synthesis results show that the proposed design yields a processing rate of about 167 M samples/second by using TSMC 0.18 m technology.

3. **HD Resolution Intra Prediction Architecture for H.264 Decoder.**
   performance video standards use prediction techniques to achieve high picture quality at low bit rates. The type of prediction decides the bit rates and the image quality. Intra Prediction achieves high video quality with significant reduction in bit rate. This paper presents novel area optimized architecture for Intra prediction of H.264 decoding at HDTV resolution. The architecture has been validated on a Xilinx Virtex-5 FPGA based platform and achieved a frame rate of 64 fps. The architecture is based on multi-level memory hierarchy to reduce latency and ensure optimum resources utilization. It removes redundancy by reusing same functional blocks across different modes. The proposed architecture uses only 13% of the total LUTs available on the Xilinx FPGA XC5VLX50T.